Electromigration Signoff Based on IR-Drop Degradation Assessment

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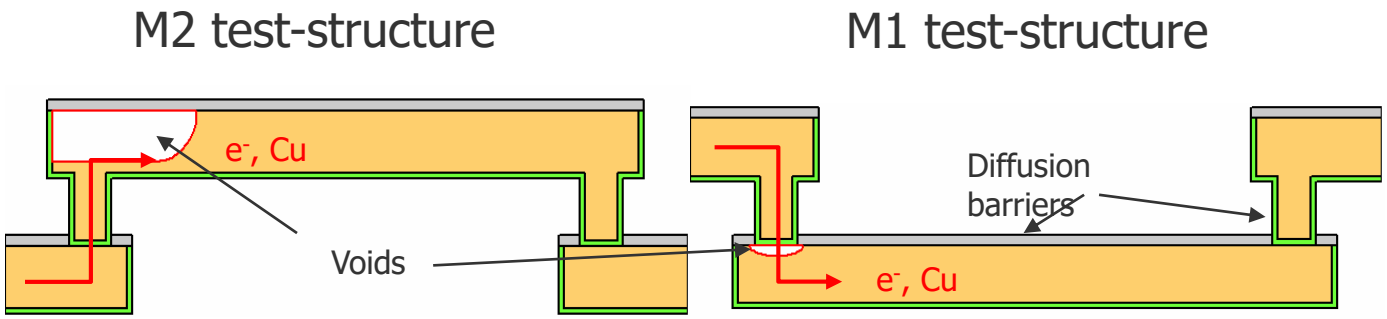
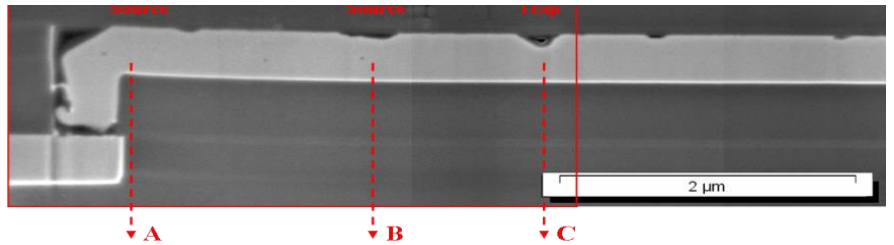
Electromigration-Induced Failures

- Electromigration is the movement of metal atoms along the wire by the applied electric current.
- When many atoms were moved out of the cathode region **voids can be formed**



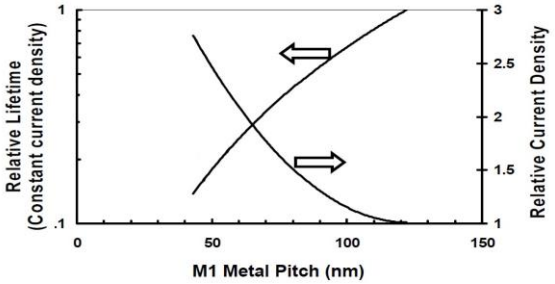


- **Voids increase resistances** of the affected metal wires.
- This can lead to undesirable changes in chip operations, for example, the timing violations can be developed.
- An intensity of void generation and, hence, a **rate of resistance degradation** can be reduced by **limiting wire electric currents**.
- Foundries introduce special design rules – **CURRENT DENSITY DESIGN RULES**, which should be obeyed in all chip designs.

Electromigration-Induced Design Problem

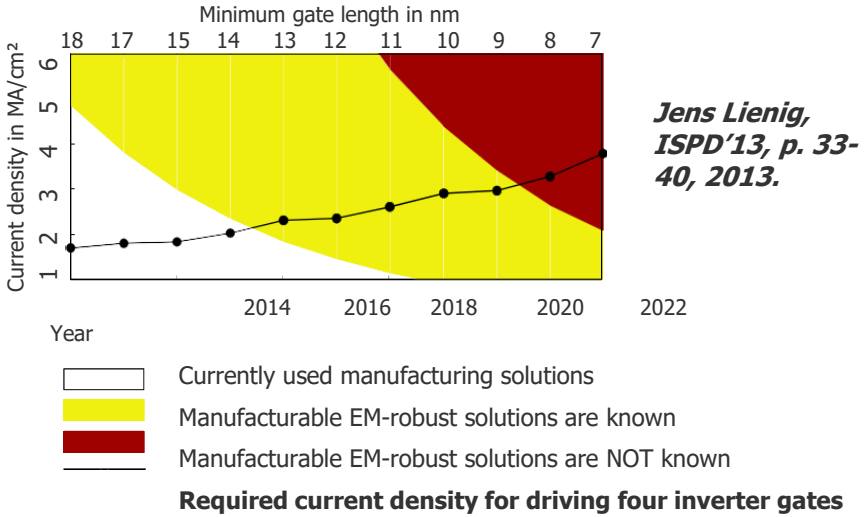
With technology scaling:

- The current densities in metal lines have been increasing
- The electromigration (EM) lifetimes of metal lines have been decreasing



With Current Circuit-Level Reliability Assessment:

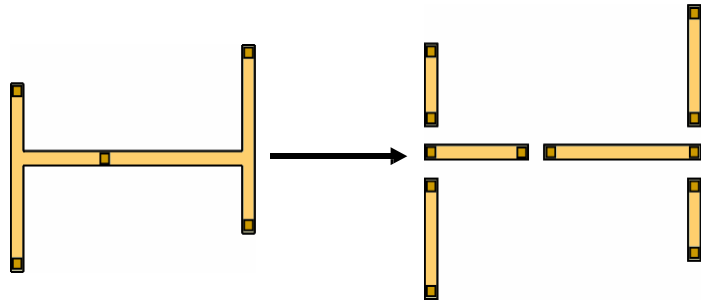
- Expected development of current densities (J_{max},) needed for driving four inverter gates, according to ITRS 2011.



Jens Lienig, ISPD'13, p. 33-40, 2013.

Current Circuit-Level Reliability Assessment:

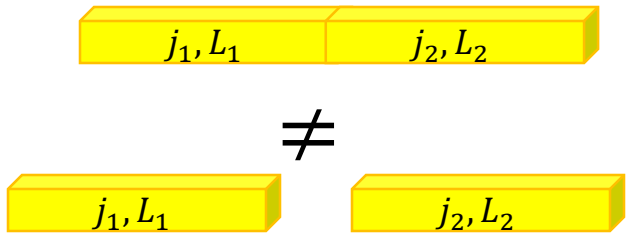
- From measured **TTF**s two parameters of Black's equation: ***n*** – a current density exponent, and E_a – an activation energy are extracted
- These parameters are used for calculating **MTTF** for other load conditions – ***j*** and ***T***
- *Decompose an interconnect layout on individual segments.*
- Remove all segments with $(jL)<(jL)_{crit}$ from further consideration.
- Calculate **MTTF** for all remaining segments.
- Assume failure occurs when shortest **MTTF** is reached.

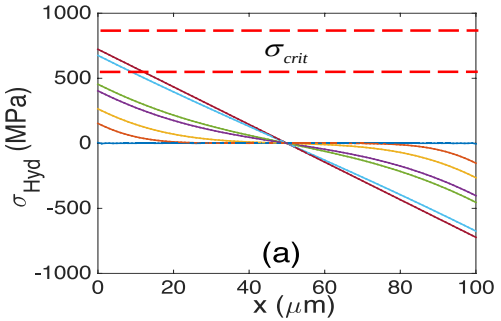


The expected lifetime of the overall system of interconnects is determined from the failure probability of the individual wire segments.

Problems with Current Approach

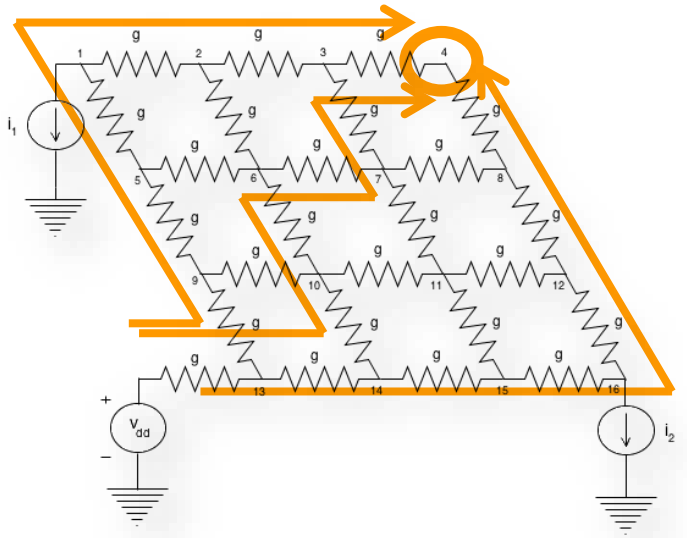
❑ Material Flow is ignored





- There are no diffusion barriers between segments of P/G, so atoms can freely flow from one segment to another.
- Thus, there is no severe atom depletion and accumulation at each segment ends.
- Voids are not expected to be formed at all segment cathode ends.

❑ Redundancy is unaccounted for

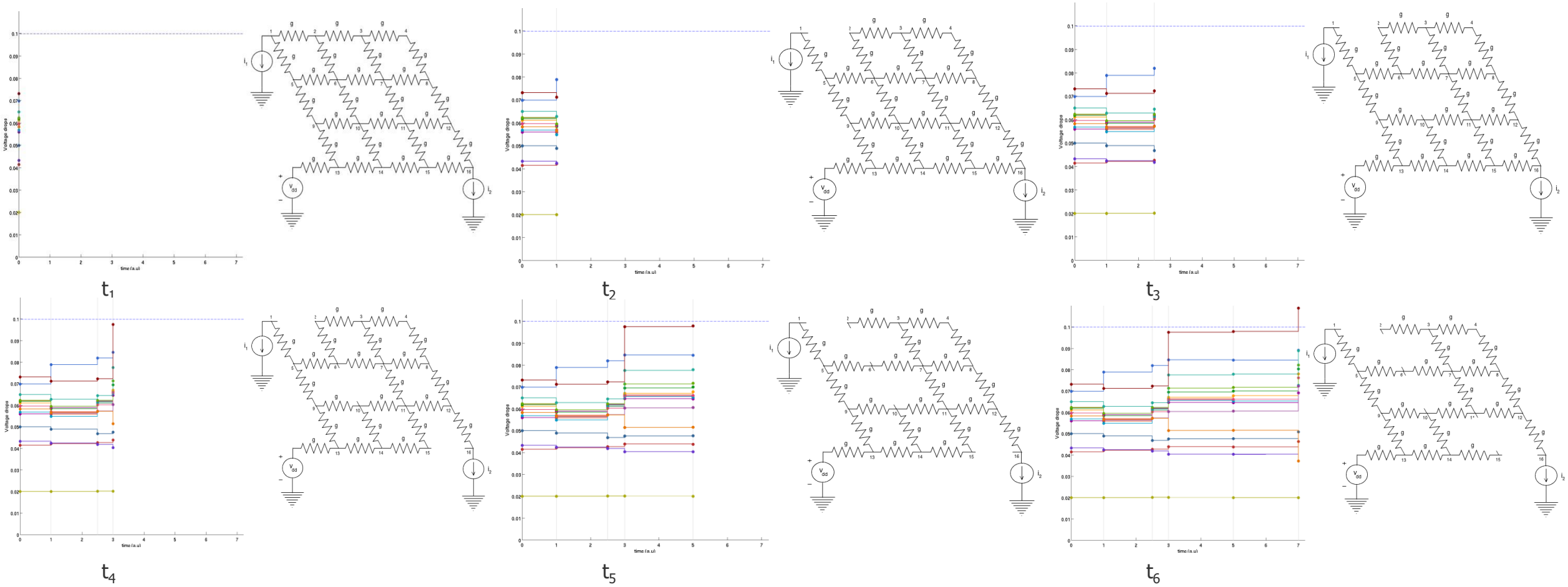


- The grid has redundancy and can survive several line failures

❑ The series model assumption.

A series model is the case where a power grid is deemed to have failed as soon as the first of its branches has failed, typically due to an open circuit. However, modern power grids use a mesh structure. As such, there are many paths for the current to flow from the flip-chip bumps to the underlying logic, a characteristic we are referred to as a redundancy. As such, it is highly pessimistic to assume that a single branch failure will always cause the whole grid to fail.

Progress Toward Failure



The key feature is that a grid is deemed to have failed, not when the first line fails, but when the voltage drop at any grid node exceeds a user specification.

Current Approach-Induced Design Problem

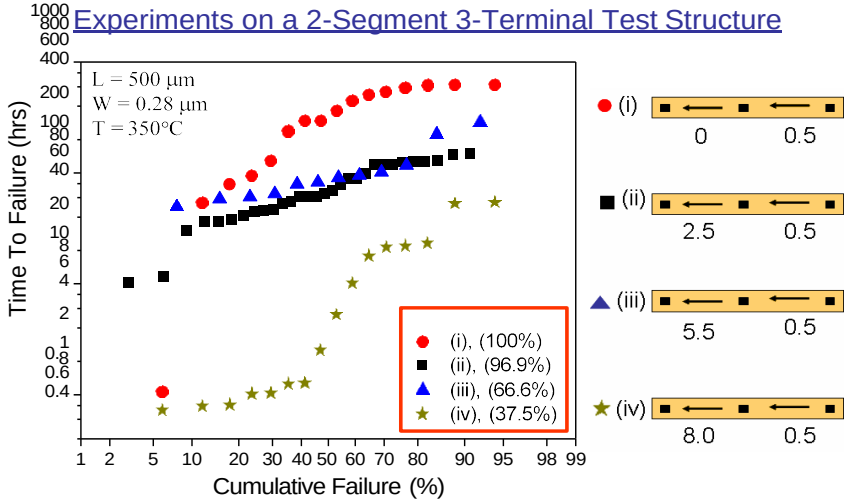
- This leads to inaccurate EM prediction during design, sometimes optimistic and often too pessimistic
  - A tree may be deemed immortal if lines are too short (Blech)
  - The grid has redundancy and can survive several line failures
- This calls for significant over-design. However, today, there is very little margin left for electromigration!
- We find that the pessimism is very high: grids that must survive 10 years, are being designed to survive ~40 years. One might think that pessimism is not a bad strategy in VLSI. However, too much pessimism in the power grid can be a big problem. It leads to overuse of metal area, leaving little room for signal routing, which makes EM signoff extremely difficult in modern designs, thus increasing design complexity and design time.
- Traditional empirical models are no longer sufficient and we need better physical models:

  A. S. Oates (TSMC) ""*… it is necessary to include electromigration-induced mechanical stresses in addition to current densities to accurately predict failure of circuit interconnects." In:*

  Interconnect reliability challenges for technology scaling: A circuit focus," in 2016 IEEE International Interconnect Technology Conference, May 2016.

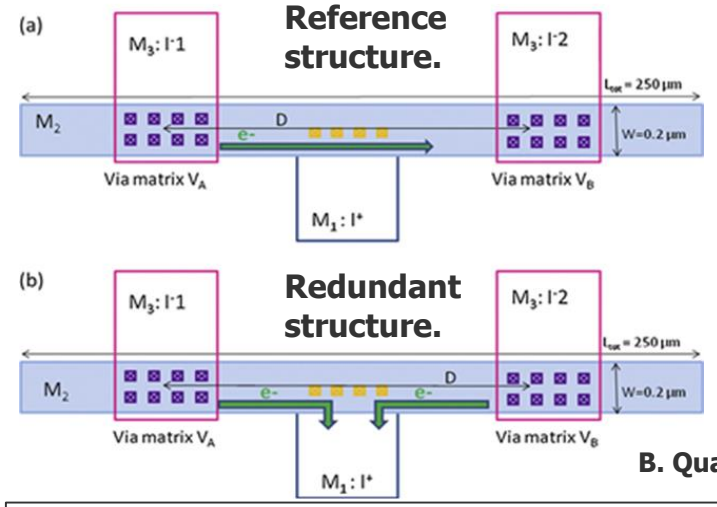
Experimental proof of role of mass transfer between segments

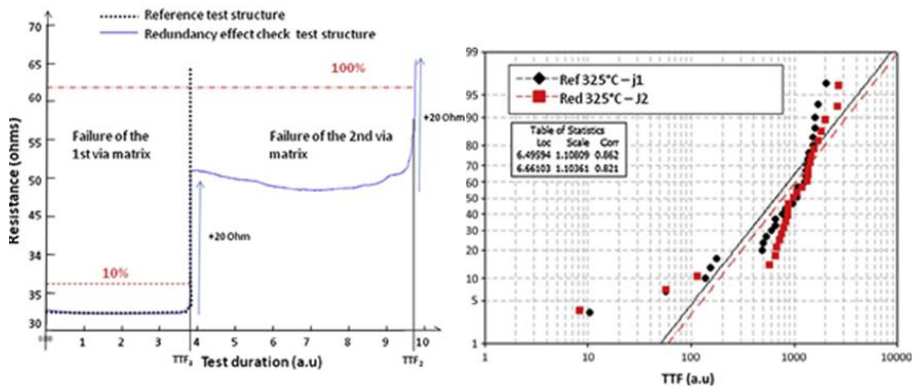
Experiments on a 2-Segment 3-Terminal Test Structure



Most failures occur in the right limb (i-iii), even though the current density is much higher in the left limb.

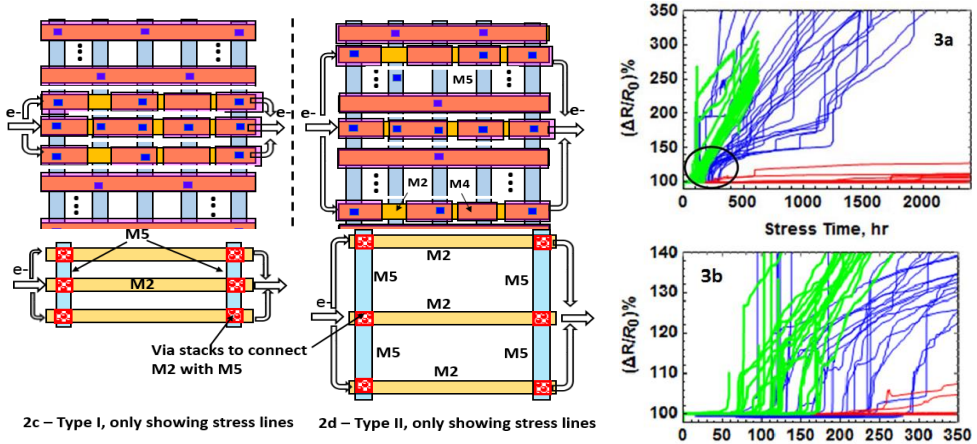
C. Gan, C. Thompson, et. Al, J. Appl. Phys. 94, 1222, 2003.



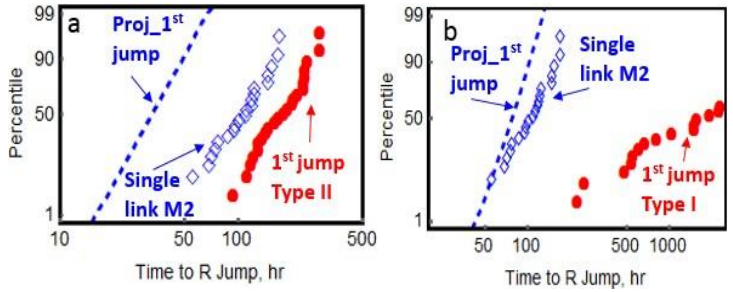


B. Quattara, L. Doyen, et al., Microelectronics Reliability, 54 (2014), 1702.

Redundant structure is characterized by two abrupt jumps of resistance, while the reference structure demonstrated just one coincident with the first jump in redundant. Same MTTF are obtained for both structures although the total current in the redundant structure is two times higher.



B. Li, A. Kim, P. McLaughlin, et al. in *IEEE IRPS Proceedings*, South San Francisco, CA, 2018, pp. 4F3.1 - 5.



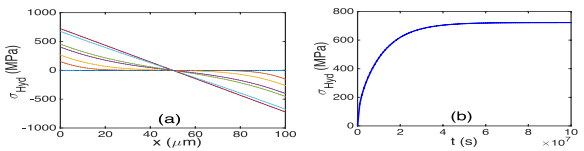
Redundancy doesn't only provide the alternative current paths, but also allows the electric current to redistribute when the EM induced void causes a local resistance increase.

Reservoir effect, which increases the EM resistance, is based on the atomic migration between the links.

EM-induced MTTF Analysis: Methodology/Tool-prototype

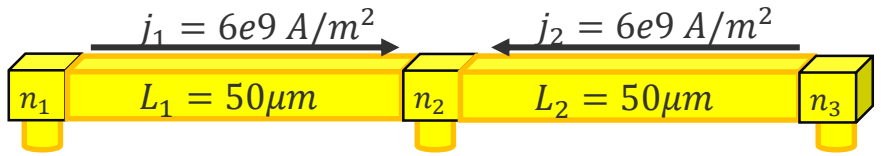
- 1-D Korhonen's model provides EM-induced stress evolution inside single-link interconnect segment:

$$\frac{\partial \sigma}{\partial t} = \frac{\partial}{\partial x}\left[\frac{D_a B \Omega}{k_B T}\left(\frac{\partial \sigma}{\partial x} + \frac{eZ^* \rho j}{\Omega}\right)\right]$$



Evolution of the hydrostatic stress (a) along the metal line loaded with DC current, and at the cathode end of line, (b) j = $5x10^9 A/m^2$, T = 400K.

- Applying Korhonen's model at every segment, combined with the boundary laws, gives a fully determined system
- Stress evolution PDE: $\frac{\partial \sigma_n}{\partial t} = \frac{\partial}{\partial x}\left[\kappa_n^2\left(\frac{\partial \sigma_n}{\partial x} + G\right)\right]$



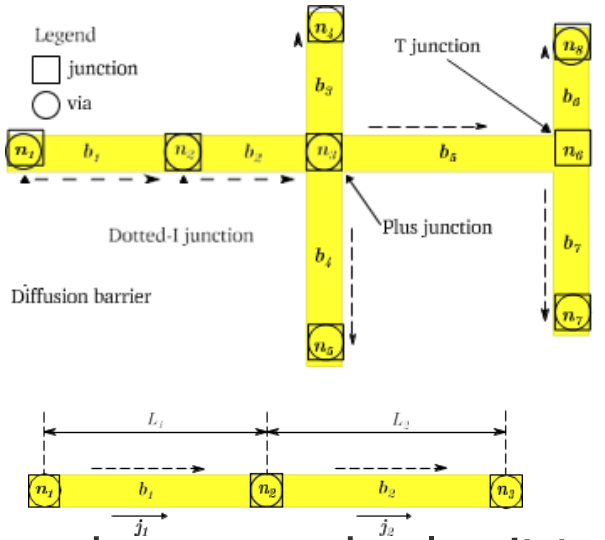
- Boundary conditions:

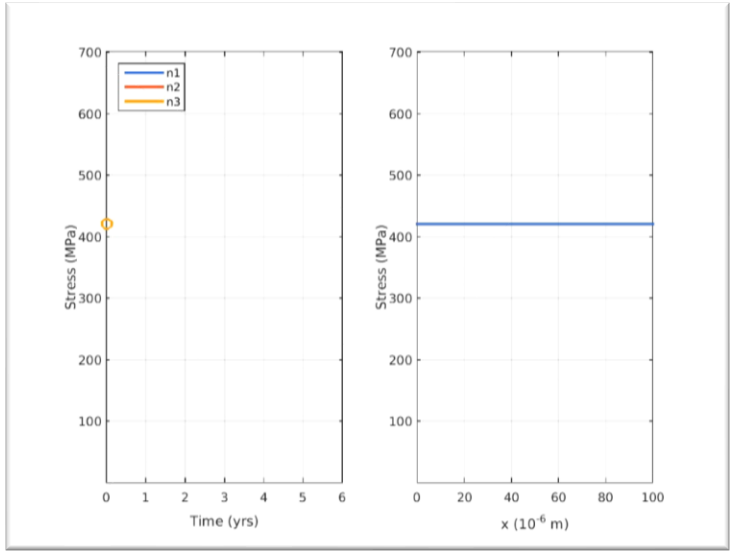
$$\sigma_n(x,t) = \sigma_{n+1}(x,t) \qquad x = x_n, t > 0$$

$$\kappa_n^2\left(\frac{\partial \sigma_n}{\partial x} + G\right) = \kappa_{n+1}^2\left(\frac{\partial \sigma_{n+1}}{\partial x} + G\right)$$

$$\frac{\partial \sigma_1}{\partial x} + G = 0 \qquad x = 0, t > 0$$

$$\frac{\partial \sigma_N}{\partial x} + G = 0 \qquad x = L, t > 0$$

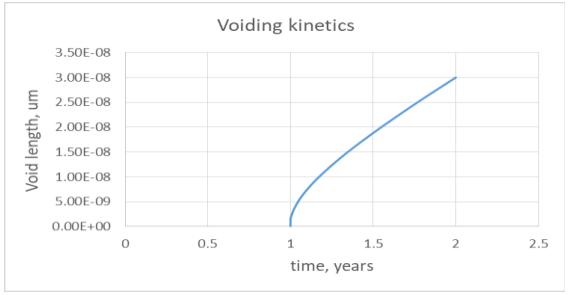


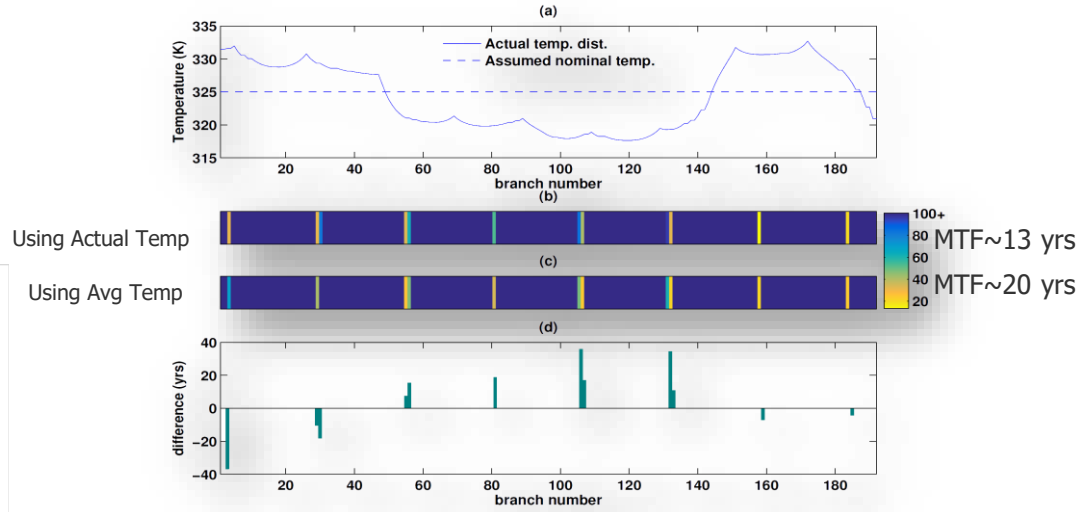


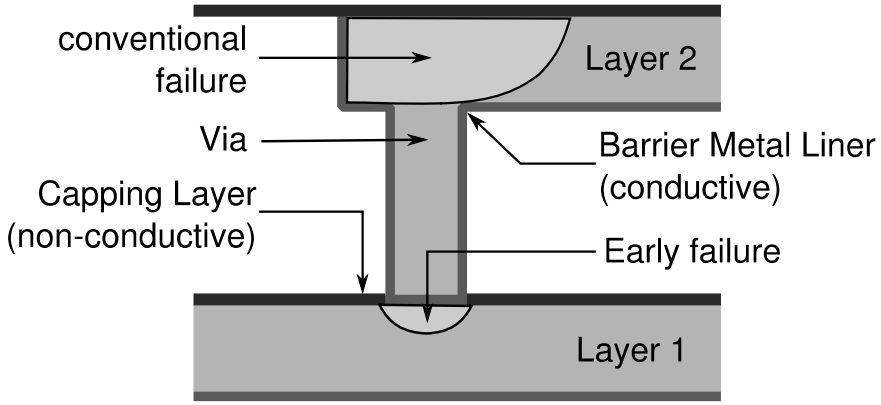
- We discretize this in time and space and solve it to give the stress evolution at every point of interconnect tree

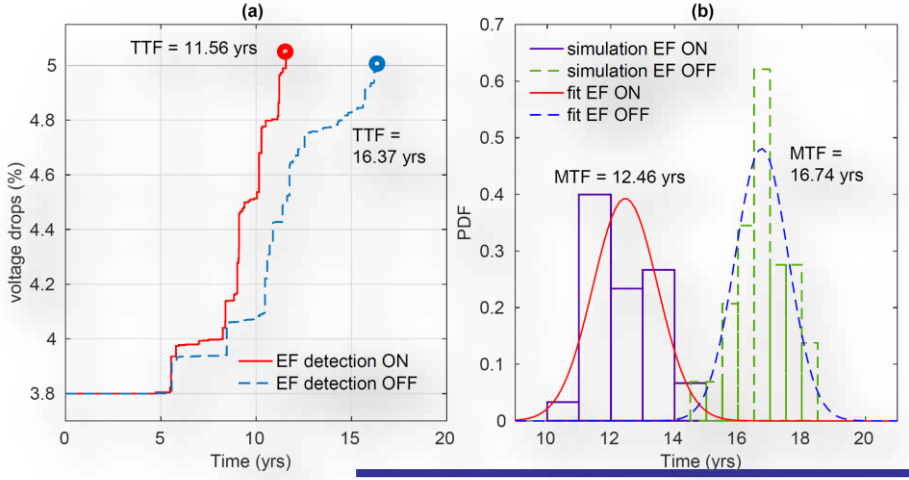
Model Features

- Effect of temperature on MTF
  - Accounting for the temperature distribution across the metal layers is done by employing a standard compact thermal model that represents a die as array of cuboidal thermal cells with effective local thermal properties.
- Voiding kinetics
  - For more accurate simulations, void growth model was implemented: after detecting void nucleation, the tool tracks void length $l_{void}(t)$
- Early failure
  - A large void right below a via can lead to an open circuit because capping layer is non-conductive: early failures.



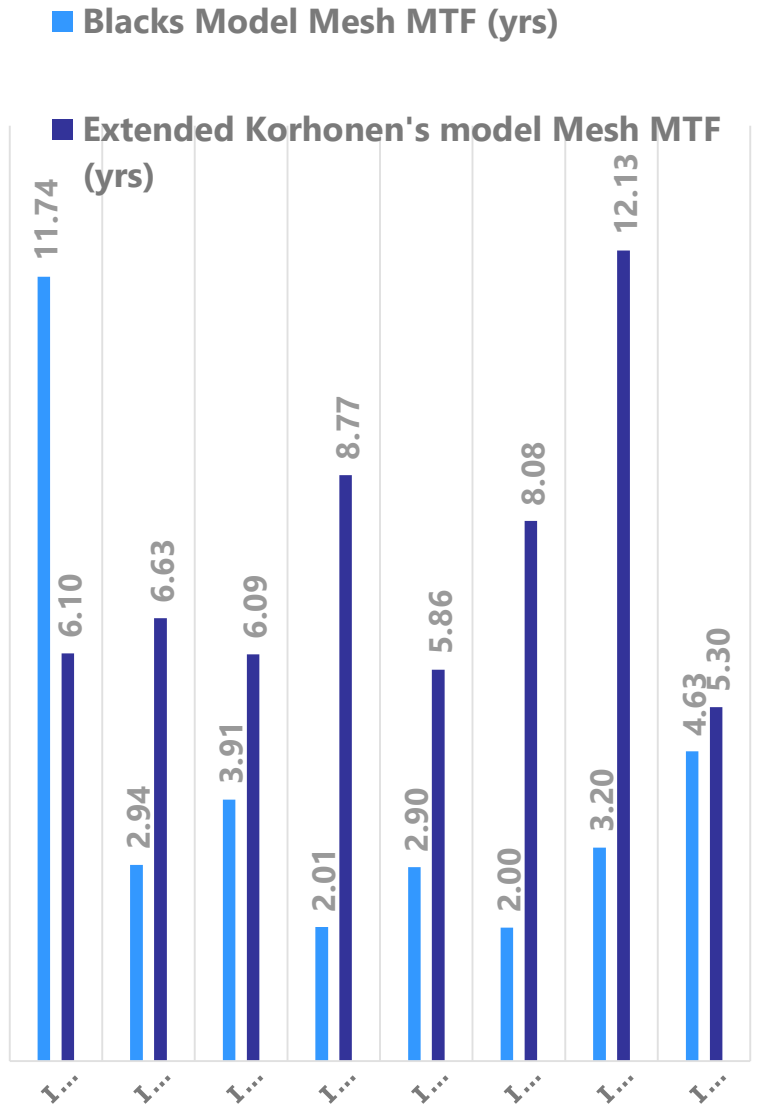






Performance / Experimental Results

Power Grids					Perform.
Grid	**# of nodes**	**# of branches**	**# of trees**	**# of current sources**	**CPU time**
Ibmpg1*	6K	11K	709	11K	0.6min
Ibmpg2*	62K	61K	462	61K	1.2min
Ibmpg3*	410K	401K	8.1K	401K	4.2min
Ibmpg4*	475K	465K	9.6K	465K	6.6min
Ibmpg5*	249K	496K	2K	496K	1.8min
Ibmpg6*	404K	798K	10.2K	798K	14.0min
Ibmpgnew1*	316K	698K	19.5K	698K	4.8min
Ibmpgnew2*	718K	698K	19.5K	698K	3.6min
Power Grid1 (65nm) 14.4x12.8 mm	13.167M	10.708M	2.459M	768	3.5h
Power Grid2 (28nm) 4.1x6.1 mm	15.520M	12.448M	2.784M	3.150M	6.5h

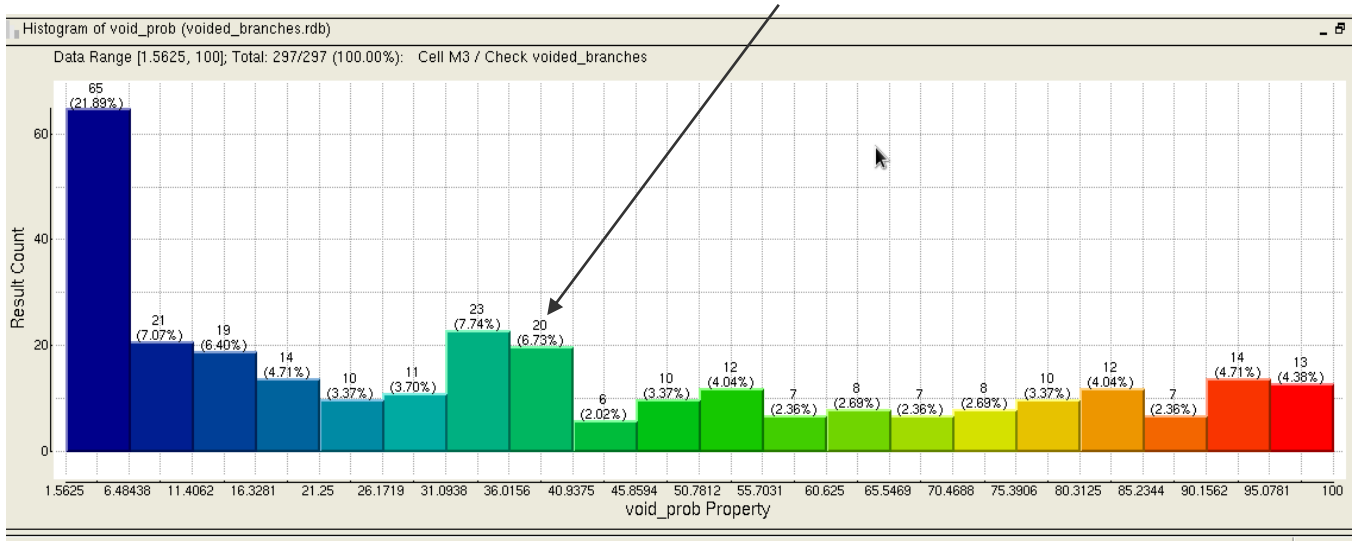


*S. R. Nassif, "Power grid analysis benchmarks," in *Proc. Asia South Pacific Design Automation Conf. (ASPDAC)* , 2008, pp. 376–381.

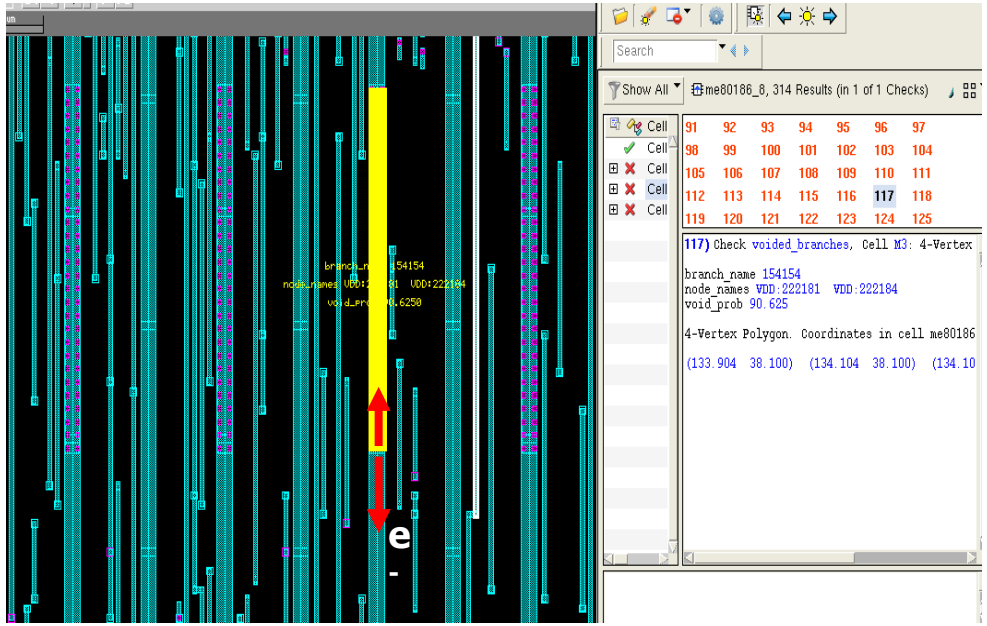
Probability of EM Voiding in Interconnect Wires

- Monte-Carlo approach allows to study the random distribution of diffusivities in wires, and to estimate the voiding probability for branches of the simulated interconnect trees.

- Each Monte-Carlo experiment provides a list of all voided branches. The lists of voided branches, generated by all performed MC iterations, allow to get voiding statistics (i.e. the voiding probability for each branch). This information is visualized in Calibre RVE.



For 20 branches voiding probability is in the range ~36 – 41%; this is 6.73% of total number of branches in M3 layer for which voiding was detected (297)

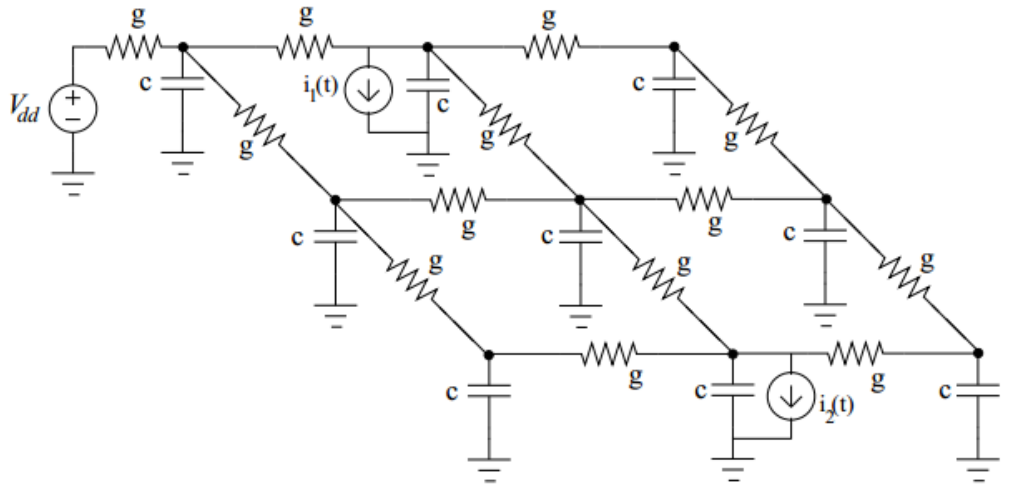


High voiding probability (P=90.625%) in the highlighted branch is due to high current inflow.

https://www.mentor.com/products/ic_nanometer_design/verification-signoff/physical-verification/calibre-rve/

CONCLUSIONS: Physics-Based EM Assessment is DEVELOPED

- Given:
  - Power Grid (DC, RC, or RLC netlist)
  - Tolerance for grid node voltage fluctuations (V_{th})
  - Effective DC for block currents
- Find:
  - Evolution of the voltage drop variations on the caused by EM induced segment resistance growth



- Features:
  - Source currents/T_0 voltage drop/Resistors are from any Power Tool (Mentor's BlueWafe).
- Results:
  - Power Grid Mean Time to Failure (MTF)
  - There are many improvements in performance, power, time-to-market and design cost that become possible if the developed physics-based EM checking is used.
- **Forward EM assessment problem is solved!**
- **Removing the over conservative foundry-based current design rules can help to extend a technology-node life-time!**